HC55185 and the IDT821054/64 Programmable Quad PCM CODEC

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Reference Design using the HC55185 and the IDT821054/64 Programmable Quad PCM CODEC

The purpose of this application note is to provide a reference design for the HC55185 and IDT821054/64 Programmable Quad PCM CODECs.

The network requirements of many countries require the analog subscriber line circuit (SLIC) to terminate the subscriber line with an impedance for voiceband frequencies which is complex, rather than resistive (e.g. 600Ω). The HC55185 accomplishes this impedance matching with a single network connected between the VTX pin and the -IN pin.

The IDT821054/64 Quad PCM CODECs uses an intergrated programmable DSP to realize AC Impedance Matching, Transhybrid Balance, Frequency Response Correction and Gain Setting functions.

Discussed in this application note are the following:

- 2-wire impedance matching.
- Receive gain (4-wire to 2-wire) and transmit gain (2-wire to 4-wire) calculations.
- Reference design for both 600Ω and 200Ω +680Ω||0.1μF (China Complex Impedance).

Impedance Matching

Impedance matching of the HC55185 to the subscriber load is important for optimization of 2 wire return loss, which in turn cuts down on echoes in the end to end voice communication path. Impedance matching of the HC55185 is accomplished by making the SLIC's impedance (Z_O, Figure 1) equal to the desired terminating impedance Z_L, minus the value of the protection resistors (R_P).

With the HC55185 programmed to match a ZL of 600Ω, the IDT821054/64 uses an intergrated programmable DSP to realize any AC impedance. The formula to program the HC55185 to match a 2-wire impedance of 600Ω is shown in Equation 1.

$$R_S = 133.3 \bullet (Z_L - 2R_P) = 133.3 \bullet (600\Omega - 2R_P) \quad \text{(EQ. 1)}$$

The value of R_S with 49Ω protection resistors is 66.9kΩ. The closest standard value is 66.5kΩ.

SLIC in the Active Mode

Figure 2 shows a simplified AC transmission model of the HC55185 and the connection of the IDT821054/64 to the SLIC. Circuit analysis of the HC55185 yields the following design equations:

The Sense Amplifier is configured as a 4 input differential amplifier with a gain of 3/4. The voltage at the output of the sense amplifier (V_{SA}) is calculated using superposition. $V_{SA}1$ is the voltage resulting from V1, $V_{SA}2$ is the voltage resulting from V2 and so on (reference Figure 2).

$$V_{SA}1 = -\frac{3}{4}(V_1) \quad \text{(EQ. 2)}$$

$$V_{SA}2 = \frac{3}{4}(V_2) \quad \text{(EQ. 3)}$$

$$V_{SA}3 = -\frac{3}{4}(V_3) \quad \text{(EQ. 4)}$$

$$V_{SA}4 = \frac{3}{4}(V_4) \quad \text{(EQ. 5)}$$

$$V_{SA} = [(V_2 - V_1) + (V_4 - V_3)]\frac{3}{4} = [\Delta V + \Delta V]\frac{3}{4} \quad \text{(EQ. 6)}$$

Where ΔV is equal to $I_M R_{SENSE}$ (R_{SENSE} = 20Ω)

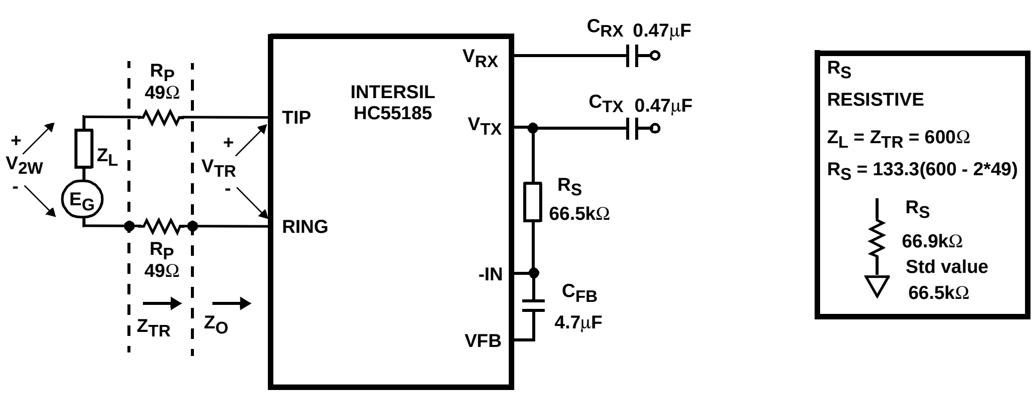
$$V_{SA} = 2(\Delta I_M \times 20)\frac{3}{4} = \Delta I_M 30 \quad \text{(EQ. 7)}$$

The voltage at VTX is equal to:

$$V_{TX} = -V_{SA}\left(\frac{R_S}{8K}\right) = -\left(\frac{R_S}{8K}\right)\Delta I_M 30 \quad \text{(EQ. 8)}$$

V_{TR} is defined in Figure 2, note polarity assigned to V_{TR}:

$$V_{TR} = 2(V_{RX} + V_{TX}) \quad \text{(EQ. 9)}$$



$Z_O = Z_L - 2R_P$

FIGURE 1. IMPEDANCE MATCHING

Setting V_{RX} equal to zero, substituting EQ. 8 into EQ. 9 and defining $Z_O = -V_{TR}/\Delta I_M$ will enable the user to determine the require feedback to match the line impedance at V_{2W}.

$$Z_O = \frac{1}{133.33} R_S \qquad \text{(EQ. 10)}$$

Z_O is the source impedance of the device and is defined as $Z_O = Z_L - 2R_p$. ZL is the line impedance. R_S is defined as:

$$R_S = 133.33(Z_L - 2R_P) \qquad \text{(EQ. 11)}$$

Node Equation at HC55185 V_{RX} input

$$I_X = \frac{V_{RX}}{R} + \frac{V_{TX}}{R} \qquad \text{(EQ. 12)}$$

Substitute Equation 8 into Equation 12

$$I_X = \frac{V_{RX}}{R} - \left(\frac{R_S \Delta I_M 30}{R8K}\right) \qquad \text{(EQ. 13)}$$

Loop Equation at HC55185 feed amplifiers and load

$$I_X R - V_{TR} + I_X R = 0 \qquad \text{(EQ. 14)}$$

Substitute Equation 13 into Equation 14

$$V_{TR} = 2V_{RX} - \left(\frac{R_S \Delta I_M 60}{8K}\right) \qquad \text{(EQ. 15)}$$

Substitute Equation 10 for R_S and $-V_{2W}/Z_L$ for ΔI_M into Equation 15.

$$V_{TR} = 2V_{RX} + \frac{Z_O V_{2W}}{Z_L} \qquad \text{(EQ. 16)}$$

Loop Equation at Tip/Ring interface

$$V_{2W} - I_M 2R_P + V_{TR} = 0 \qquad \text{(EQ. 17)}$$

Substitute Equation16 into Equation 17 and combine terms

$$V_{2W}\left[\frac{Z_L + Z_O + 2R_P}{Z_L}\right] = -2V_{RX} \qquad \text{(EQ. 18)}$$

where:

V_{RX} = The input voltage at the V_{RX} pin.

V_{SA} = An internal node voltage that is a function of the loop current and the output of the Sense Amplifier.

I_X = Internal current in the SLIC that is the difference between the input receive current and the feedback current.

I_M = The AC metallic current.

R_P = A protection resistor (typical 49.9Ω).

R_S = An external resistor/network for matching the line impedance.

V_{TR} = The tip to ring voltage at the output pins of the SLIC.

V_{2W} = The tip to ring voltage including the voltage across the protection resistors.

Z_L = The line impedance.

Z_O = The source impedance of the device.

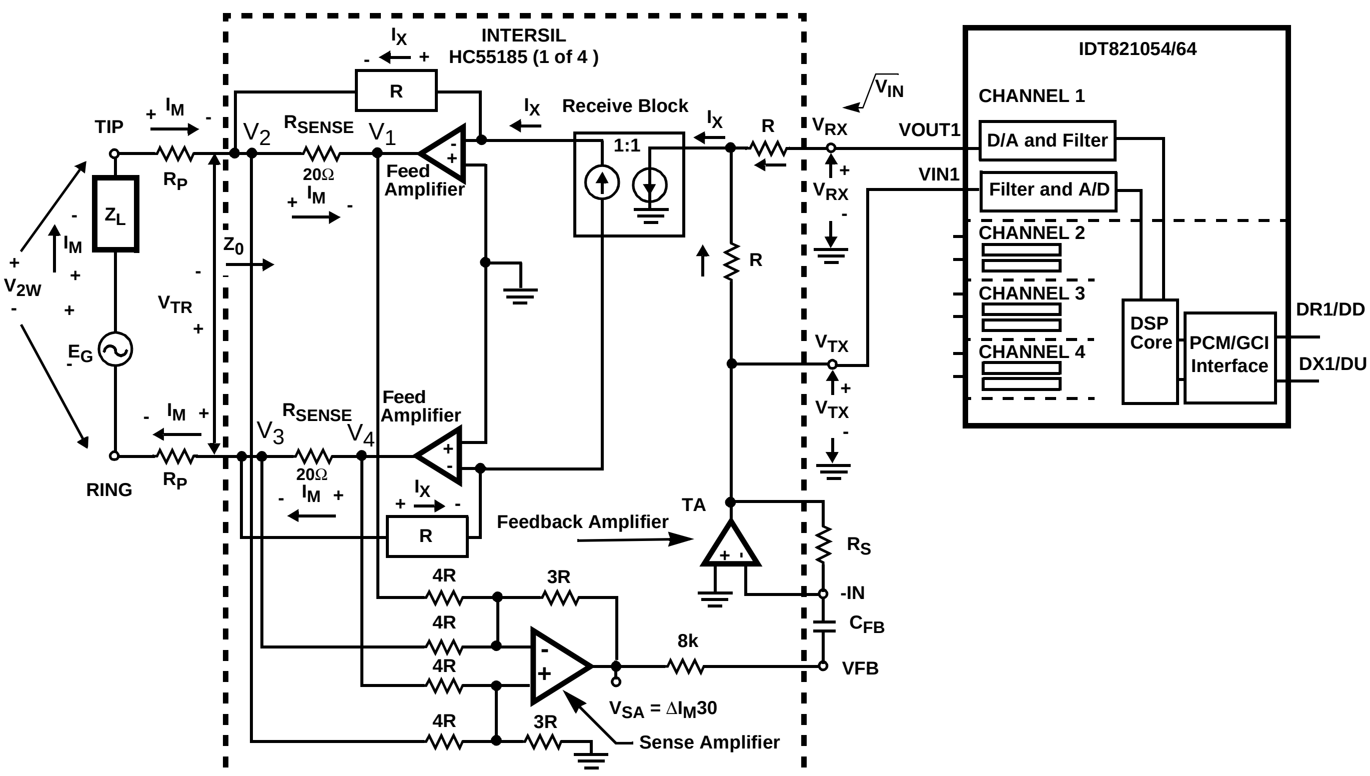


FIGURE 2. HC55185 SIMPLIFIED AC TRANSMISSION CIRCUIT AND IDT821054/64

HC55185 Receive Gain (V_{RX} to V_{2W})

4-wire to 2-wire gain across the HC55185 is equal to the V_{2W} divided by the input voltage V_{RX}, reference Figure 2. The receive gain is calculated using Equation 18.

Equation 19 expresses the receive gain (V_{RX} to V_{2W}) in terms of network impedances. From Equation 11, the value of R_S was set to match the line impedance (Z_L) to the HC55185 plus the protection resistors (Z_0 + $2R_P$). This results in a 4-wire to 2-wire gain of -1, as shown in EQ19.

$$G_{4\text{-}2} = \frac{V_{2W}}{V_{RX}} = -2\frac{Z_L}{Z_L + Z_O + 2_{RP}} = -2\frac{Z_L}{Z_L + Z_L} = -1 \qquad \text{(EQ. 19)}$$

Receive Gain Across the System

The receive gain across the system is defined as the gain from the PCM highway to the phone (V_{2W}). With the receive gain through the HC55185 set to 1, the receive gain across the system is entirely controlled by programming the IDT821054/64. The IDT821054/64 can program the receive gain across the system in two ways (reference Figure 3).

- The first is by programming the signal gain in its analog form. The analog receive gain, also known as Digital to Analog (D/A) gain, can be programmed in the IDT821054/64 to be either 0dB or -6dB.
- The second is by programming the signal gain (via. coefficients) when its in digital form. The digital form of the receive path can be programmed from +3 to -12dB with minimum 0.1dB steps.

This results in a possible receive gain (D/A) programming range from +3dB to -18dB. ***Note: Analog gain brings less noise than digital gain. When allocating the CODEC gain, the majority of the required gain should be preformed in the analog stage.***

Reference section titled “Information Required for IDT to Calculate IDT821054/64 CODEC DSP Coefficients” for information on obtaining coefficients for your design.

Transmit Gain Across HC55185 (E_G to V_{TX})

The 2-wire to 4-wire gain is equal to V_{TX}/E_G with V_{RX} = 0, reference Figure 2.

Loop Equation

$$-E_G + Z_L I_M + 2R_P I_M - V_{TR} = 0 \qquad \text{(EQ. 20)}$$

From Equation 16 with V_{RX} = 0

$$V_{TR} = \frac{Z_O V_{2W}}{Z_L} \qquad \text{(EQ. 21)}$$

Substituting Equation 21 into Equation 20 and simplifying.

$$E_G = -V_{2W}\left[\frac{Z_L + 2R_P + Z_O}{Z_L}\right] \qquad \text{(EQ. 22)}$$

Substituting Equation 10 into Equation 8 and defining $\Delta I_M = -V_{2W}/Z_L$ results in Equation 23 for VTX.

$$V_{TX} = \frac{V_{2W}}{2}\left[\frac{Z_L - 2R_P}{Z_L}\right] \qquad \text{(EQ. 23)}$$

Combining Equations 22 and 23 results in Equation 24.

$$G_{2\text{-}4} = \frac{V_{TX}}{E_G} = -\frac{Z_L - 2R_P}{2(Z_L + 2R_P + Z_O)} = -\frac{Z_O}{2(Z_L + 2R_P + Z_O)} \qquad \text{(EQ. 24)}$$

A more useful form of the equation is rewritten in terms of V_{TX}/V_{2W}. A voltage divider equation is written to convert from E_G to V_{2W} as shown in Equation 25.

$$V_{2W} = \left(\frac{Z_O + 2_{RP}}{Z_L + Z_O + 2_{RP}}\right)E_G \qquad \text{(EQ. 25)}$$

Substituting $Z_L = Z_O + 2_{RP}$ and rearranging Equation 25 in terms of E_G results in Equation 26.

$$E_G = 2V_{2W} \qquad \text{(EQ. 26)}$$

Substituting Equation 26 into Equation 24 results in an equation for 2-wire to 4-wire gain that’s a function of the synthesized input impedance of the SLIC and the protection resistors.

$$G_{2\text{-}4} = \frac{V_{TX}}{V_{2W}} = -\frac{Z_O}{(Z_L + 2R_P + Z_O)} = 0.416 \qquad \text{(EQ. 27)}$$

Z_L is set to 600Ω, Z_O is programmed with R_S to be 498.76Ω (66.5kΩ/133.33), and R_P is equal to 49.9Ω. This results in a 2-wire to 4-wire gain of 0.416 or -7.6dB.

Transmit Gain Across the System

The transmit gain across the system is defined as the gain from the phone or 2-wire side (V_{2W}) to the PCM highway. Setting the gain of the IDT821054/64 will have to account for the attenuated signal through the HC55185. The system gain is entirely controlled by programming the IDT821054/64. The IDT821054/64 can program the transmit gain across the system in two ways (reference Figure 3).

- The first is by programming the signal gain in its analog form. The analog transmit gain, also known as Analog to Digital (A/D) gain, can be programmed in the IDT821054/64 to be either 0dB or +6dB.
- The second is by programming the signal gain (via. coefficients) when its in digital form. The digital form of the transmit path can be programmed from -3dB to +12dB with minimum 0.1dB steps.

This results in a possible transmit gain (A/D) programming range from -3dB to +18dB. ***Note: Analog gain brings less noise than digital gain. When allocating the CODEC gain, the majority of the required gain should be preformed in the analog stage.***

Reference section titled “Information Required for IDT to Calculate IDT821054/64 CODEC DSP Coefficients” for information on obtaining coefficients for your design.

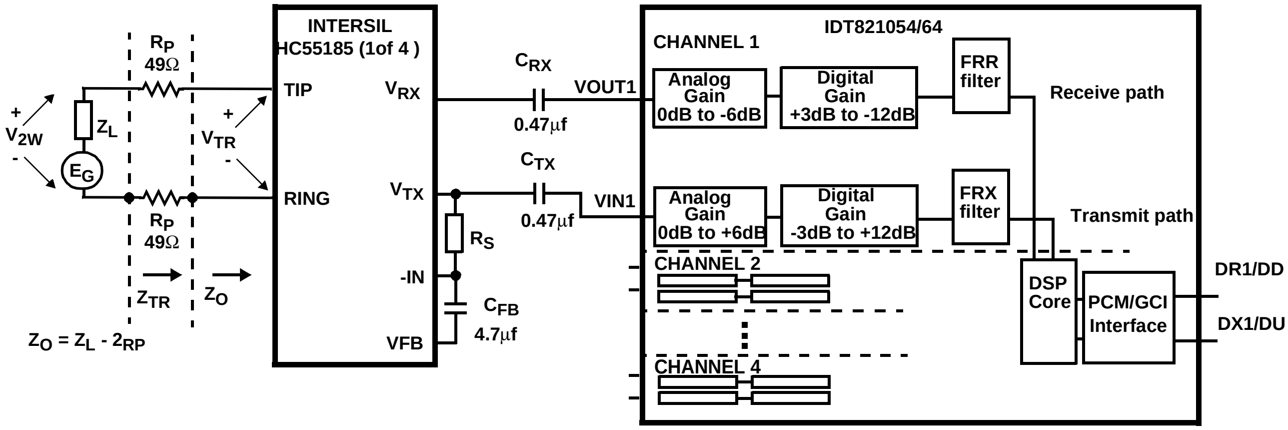


FIGURE 3. RECEIVE GAIN G(4-2), TRANSMIT GAIN (2-4)

Transhybrid Balance G(4-4)

Transhybrid balance is a measure of how well the input signal is canceled (that being received by the SLIC) from the transmit signal (that being transmitted from the SLIC to the CODEC). Without this function, voice communication would be difficult because of the echo. The Transhybrid balancing filter inside the IDT821054/64 is used to adjust transhybrid balance to ensure the echo cancellation meets the ITU-T specifications. The coefficient for Echo Cancellation is ECF.

Frequency Response Correction

The FRR filter in the receive path and the FRX filter in the transmit path can be programmed to correct any frequency distortion caused by the impedance matching filters. The coefficients of Frequency Response Correction are FRR for receive path and FRX for the transmit path.

Information Required for IDT to Calculate IDT821054/64 CODEC DSP Coefficients

For IDT to calculate IDT821054/64 DSP coefficient, customers should provide the following information about their subscriber line card:

- Accurate SLIC PSPICE model. It can be provided in .lib file or PSPICE schematic file.
- System Impedance
- Gain (Transmit path and Receive path)

Using the DSP coefficients provided by IDT, the overall performance of the system will pass ITU-T requirements.

When the COF RAM button is selected from the MPI Operation General Interface screen, the COF RAM Operation screen will appear (Figure 4). From this screen, the user can configure all the coefficients for the current channel.

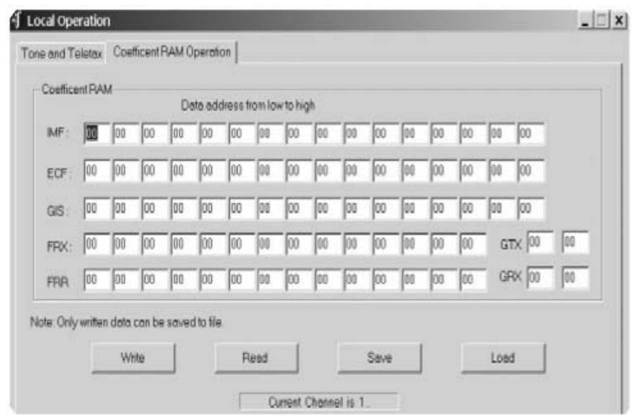


FIGURE 4. COEFFICIENT RAM OPERATION SCREEN

Reference Design of the HC55185 and the IDT821054/64 With a 600Ω Load

The design criteria is as follows:

- 4-wire to 2-wire gain (DR1/DD to V_{2W}) equal 0dB
- 2-wire to 4-wire gain (V_{2W} to DX1/DU) equal 0dB
- Rp = 49.9Ω

Figure 5 gives the reference design using the Intersil HC55185 and the IDT821054/64 Programmable Quad PCM CODEC. Also shown in Figure 5 are the voltage levels at specific points in the circuit.

Impedance Matching

The 2-wire impedance is matched to the line impedance Z_0 using Equation 1, repeated here in Equation 28.

$$R_S = 133.3 \bullet (Z_L - 2R_P) \qquad \text{(EQ. 28)}$$

For a line impedance of 600Ω, R_S equals:

$$R_S = 133.3 \bullet (600 - 98) = 66.9k\Omega \qquad \text{(EQ. 29)}$$

The closest standard value for R_S would be 66.5kΩ.

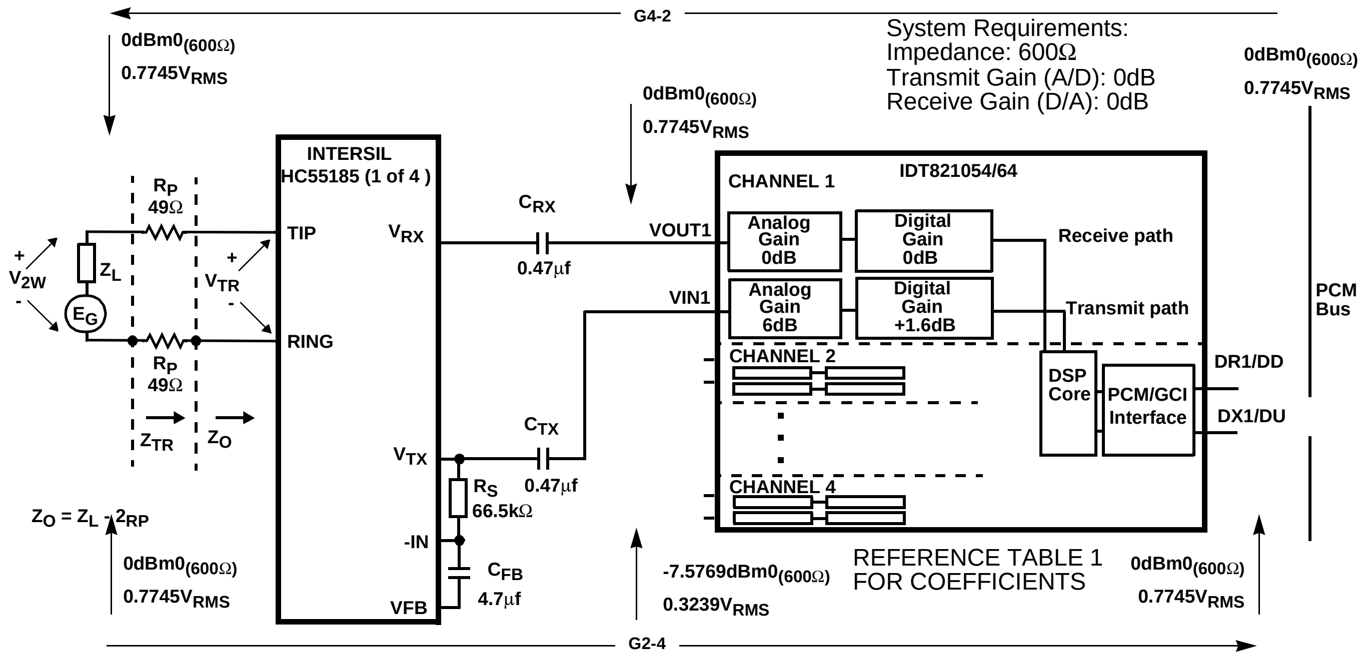


FIGURE 5. REFERENCE DESIGN OF THE HC55185 AND THE IDT821054/64 WITH A 600Ω LOAD IMPEDANCE

However, it would be very convenient and cost effective if system manufacturers can use only one type of line card to meet different impedance requirements and different gain requirements. The programmability of IDT821054/64 can help system manufactures to reach this goal. By using different coefficients this reference design can meet both 600Ω and $200\Omega + 680\Omega \| 0.1\mu$ F impedance requirements.

With the value of R_S selected to be $66.5k\Omega \pm 1\%$, the coefficients (with a line impedance of 600Ω) are given in Table 1.

Specific Implementation for China

The design criteria for a China specific solution are as follows:

- Desired line circuit impedance is 200 + 680//0.1μF
- Receive gain (V_{2W}/(DR1/DD)) is -3.5dB
- Transmit gain ((DX1/DU)/V_{2W}) is 0dB
- 0dBm0 is defined as 1mW into the complex impedance at 1020Hz
- R_p = 49.9Ω

Figure 6 gives the reference design using the Intersil HC55185 and the IDT821054/64 Programmable Quad PCM CODEC. Also shown in Figure 6 are the voltage levels at specific points in the circuit. Note: The transmit gain of the system is 0dB (-2.19dB$_{(811\Omega)}$ = -3.5dB$_{(600\Omega)}$) as explained in the following section.

Adjustment to Get -3.5dBm0 at the Load Referenced to 600Ω

The voltage equivalent to 0dBm0 into 811Ω (0dBm0$_{(811\Omega)}$) is calculated using Equation 30 (811Ω is the impedance of complex China load at 1020Hz).

$$0dBm_{(811\Omega)} = 10\log\frac{V^2}{811(0.001)} = 0.90055V_{RMS} \quad \text{(EQ. 30)}$$

The gain referenced back to 0dBm0$_{(600\Omega)}$ is equal to:

$$GAIN = 20\log\frac{0.90055V_{RMS}}{0.7745V_{RMS}} = 1.309dB \quad \text{(EQ. 31)}$$

The adjustment to get -3.5dBm0 at the load referenced to 600Ω is:

$$Adjustment = -3.5dBm0 + 1.309dBm0 = -2.19dB \quad \text{(EQ. 32)}$$

The voltage at the load (referenced to 600Ω) is given in Equation 33:

$$-2.19dBm_{(600\Omega)} = 10\log\frac{V^2}{600(0.001)} = 0.60196V_{RMS} \quad \text{(EQ. 33)}$$

Impedance Matching

With the value of R_S selected to be $66.5k\Omega \pm 1\%$, the coefficients (with a line impedance of $200\Omega + 680\Omega \| 0.1\mu$ F) are given in Table 2.

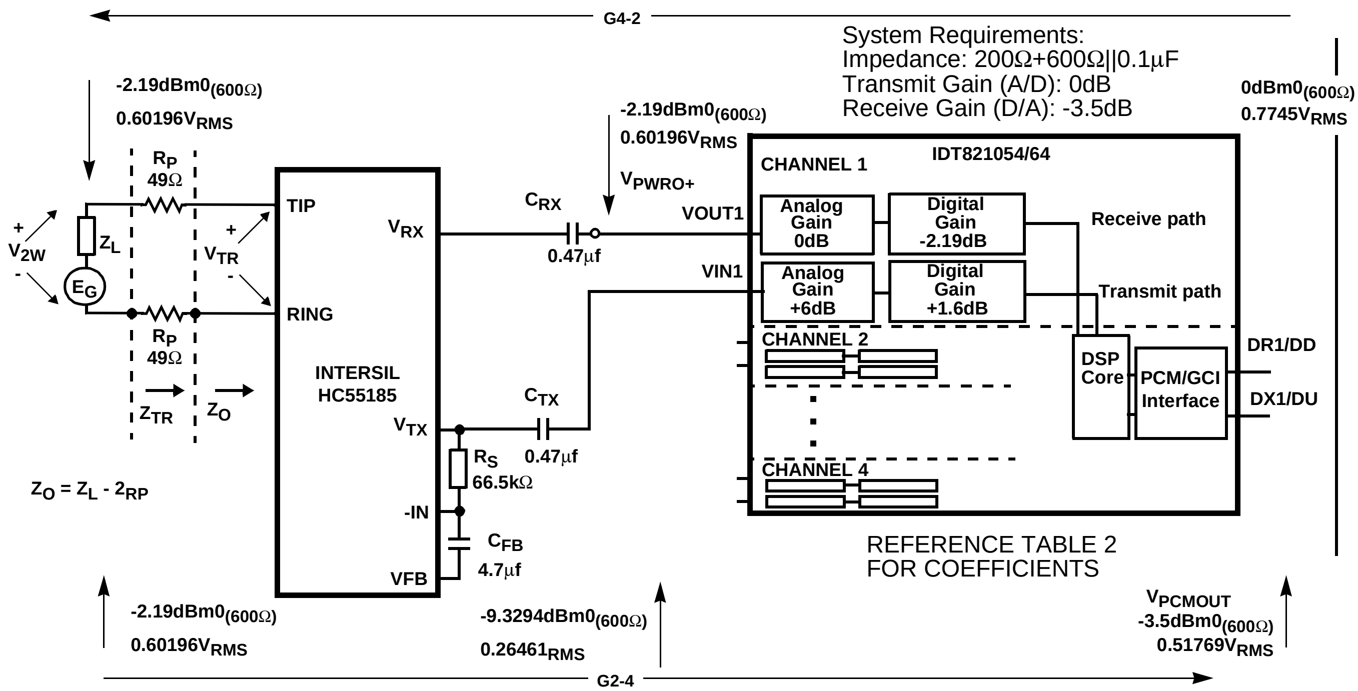


FIGURE 6. REFERENCE DESIGN OF THE HC55185 AND THE IDT821054/64 WITH CHINA COMPLEX LOAD IMPEDANCE

TABLE 1. 600Ω COEFFICIENTS, SYSTEM GAINS: (TRANSMIT GAIN (0dB), RECEIVE GAIN (0dB)), CODEC ANALOG GAINS: (TRANSMIT PATH +6dB, RECEIVE PATH 0dB)

Coefficient RAM				**CHANNEL 1**													
IMF:	47	08	53	F5	00	00	00	00	00	00	00	00	00	00	00	00	
ECF:	3C	03	00	00	00	00	00	00	00	00	56	62	F4	D6	00	00	
KM:	00	00	34	E6	00	00	00	00	00	00	00	00	00	00	00	00	
ACT:	36	02	97	DE	95	48	95	48	97	DE	36	02	99	31	***GTX***	FF	1F
ACR:	F8	00	55	FD	70	3F	70	3F	55	FD	F8	00	CE	84	***GRX***	0C	03
Coefficient RAM				**CHANNEL 2**													
IMF:	47	08	53	F5	00	00	00	00	00	00	00	00	00	00	00	00	
ECF:	3C	03	00	00	00	00	00	00	00	00	56	62	F4	D6	00	00	
KM:	00	00	34	E6	00	00	00	00	00	00	00	00	00	00	00	00	
ACT:	36	02	97	DE	95	48	95	48	97	DE	36	02	99	31	***GTX***	FF	1F
ACR:	F8	00	55	FD	70	3F	70	3F	55	FD	F8	00	CE	84	***GRX***	0C	03
Coefficient RAM				**CHANNEL 3**													
IMF:	47	08	53	F5	00	00	00	00	00	00	00	00	00	00	00	00	
ECF:	3C	03	00	00	00	00	00	00	00	00	56	62	F4	D6	00	00	
KM:	00	00	34	E6	00	00	00	00	00	00	00	00	00	00	00	00	
ACT:	36	02	97	DE	95	48	95	48	97	DE	36	02	99	31	***GTX***	FF	1F
ACR:	F8	00	55	FD	70	3F	70	3F	55	FD	F8	00	CE	84	***GRX***	0C	03

TABLE 1. 600Ω COEFFICIENTS, SYSTEM GAINS: (TRANSMIT GAIN (0dB), RECEIVE GAIN (0dB)), CODEC ANALOG GAINS: (TRANSMIT PATH +6dB, RECEIVE PATH 0dB) (Continued)

Coefficient RAM				CHANNEL 4													
IMF:	47	08	53	F5	00	00	00	00	00	00	00	00	00	00	00	00	
ECF:	3C	03	00	00	00	00	00	00	00	00	56	62	F4	D6	00	00	
KM:	00	00	34	E6	00	00	00	00	00	00	00	00	00	00	00	00	
ACT:	36	02	97	DE	95	48	95	48	97	DE	36	02	99	31	***GTX***	FF	1F
ACR:	F8	00	55	FD	70	3F	70	3F	55	FD	F8	00	CE	84	***GRX***	0C	03

TABLE 2. 200Ω + 680Ω || 0.1μF COEFFICIENTS, SYSTEM GAINS: (TRANSMIT GAIN (0dB), RECEIVE GAIN (-3.5dB)), CODEC ANALOG GAINS: (TRANSMIT PATH +6dB, RECEIVE PATH 0dB))

COEFFICIENT RAM				CHANNEL 1													
IMF:	52	F8	20	1D	00	00	00	00	22	65	00	00	00	00	00	00	
ECF:	0B	03	00	00	00	00	00	00	00	00	36	72	29	C2	00	00	
KM:	00	00	74	C6	00	00	00	00	00	00	00	00	00	00	00	00	
ACT:	C9	FE	9C	10	D4	45	D4	45	9C	10	C9	FE	00	38	***GTX***	FF	1F
ACR:	0A	FA	1D	0D	AF	39	AF	39	1D	0D	0A	FA	CE	84	***GRX***	0C	03
COEFFICIENT RAM				**CHANNEL 2**													
IMF:	52	F8	20	1D	00	00	00	00	22	65	00	00	00	00	00	00	
ECF:	0B	03	00	00	00	00	00	00	00	00	36	72	29	C2	00	00	
KM:	00	00	74	C6	00	00	00	00	00	00	00	00	00	00	00	00	
ACT:	C9	FE	9C	10	D4	45	D4	45	9C	10	C9	FE	00	38	***GTX***	FF	1F
ACR:	0A	FA	1D	0D	AF	39	AF	39	1D	0D	0A	FA	CE	84	***GRX***	0C	03
COEFFICIENT RAM				**CHANNEL 3**													
IMF:	52	F8	20	1D	00	00	00	00	22	65	00	00	00	00	00	00	
ECF:	0B	03	00	00	00	00	00	00	00	00	36	72	29	C2	00	00	
KM:	00	00	74	C6	00	00	00	00	00	00	00	00	00	00	00	00	
ACT:	C9	FE	9C	10	D4	45	D4	45	9C	10	C9	FE	00	38	***GTX***	FF	1F
ACR:	0A	FA	1D	0D	AF	39	AF	39	1D	0D	0A	FA	CE	84	***GRX***	0C	03
COEFFICIENT RAM				**CHANNEL 4**													
IMF:	52	F8	20	1D	00	00	00	00	22	65	00	00	00	00	00	00	
ECF:	0B	03	00	00	00	00	00	00	00	00	36	72	29	C2	00	00	
KM:	00	00	74	C6	00	00	00	00	00	00	00	00	00	00	00	00	
ACT:	C9	FE	9C	10	D4	45	D4	45	9C	10	C9	FE	00	38	***GTX***	FF	1F
ACR:	0A	FA	1D	0D	AF	39	AF	39	1D	0D	0A	FA	CE	84	***GRX***	0C	03